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Semiconductor Processing Methods Of Forming A Conductive Projection And Methods Of Increasing Alignment Tolerances

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INVENTORS

Mark Fischer
John K. Zahurak
Thomas M. Graettinger
Kunal R. Parekh

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SEMICONDUCTOR PROCESSING METHODS OF FORMING A CONDUCTIVE PROJECTION AND METHODS OF INCREASING ALIGNMENT TOLERANCES

TECHNICAL FIELD

This invention relates to semiconductor processing methods of forming conductive projections, and to methods of increasing alignment tolerances.

BACKGROUND OF THE INVENTION

As dimensions of semiconductor devices continue to shrink, alignment of individual device components, and compensation for misalignment become increasingly important. Problems associated with feature misalignment can cause shorting and other catastrophic device failure.

In forming semiconductor devices, it is not uncommon to use a conductive projection of material such as a conductive plug to form an intermediate electrical connection between a substrate node location and a device component. An exemplary conductive projection is shown in Figs. 1-3.

Referring to Fig. 1, a semiconductor wafer fragment is shown generally at 20 and comprises a semiconductive substrate 22. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a

semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A pair of isolation oxide regions 24 are formed over substrate 22. A plurality of conductive lines 26 are provided and typically include a polysilicon layer 28, a silicide layer 30 and an insulative cap 32. Sidewall spacers 34 are provided over conductive and non-conductive portions of line 26. Diffusion regions 35 are provided and constitute node locations with which electrical communication is desired. Wafer fragment 20 comprises a portion of a dynamic random access memory (DRAM) device. Conductive projections 36 are provided. A centermost of the conductive projections 36 is positioned to establish electrical communication between diffused regions and a bit line yet to be formed. The conductive projections are typically formed within an opening in an insulative oxide layer such as borophosphosilicate glass (BPSG), and subsequently planarized. A layer 38 is formed over substrate 22 and comprises an insulative material such as BPSG.

Referring to Fig. 2, a pair of contact openings 40 are formed through layer 38 and outwardly expose the illustrated projections 36. Contact openings 40 constitute openings within which storage capacitors are to be formed. Such capacitors are typically formed by providing a layer of conductive material within opening 40 and over layer 38, and

subsequently depositing a capacitor dielectric layer and cell plate layer thereover.

Referring to Fig. 3, an enlarged portion of Fig. 2 shows an example alignment tolerance X between centermost conductive projection 36 and a dashed extension of the right edge of one opening 40. A misalignment of the mask used to form contact opening 40 which is greater than X, and in the direction of the conductive projection, can result in overlap of contact opening 40 and centermost conductive projection 36. Such would subsequently cause conductive capacitor material provided into contact opening 40 to be shorted with centermost conductive projection 36 thereby rendering this portion of the device inoperative.

This invention arose out of concerns associated with increasing alignment tolerances between conductive projections and electrical components formed over a semiconductor wafer. The artisan will appreciate other applicability, with the invention only being limited by the accompanying claims appropriately interpreted in accordance with the doctrine of equivalents.

SUMMARY OF THE INVENTION

Semiconductor processing methods of forming conductive projections and methods of increasing alignment tolerances are described. In one implementation, a conductive projection is formed over a substrate surface area and includes an upper surface and a side surface joined

therewith to define a corner region. The corner region of the conductive projection is subsequently beveled to increase an alignment tolerance relative thereto. In another implementation, a conductive plug is formed over a substrate node location between a pair of conductive lines and has an uppermost surface. Material of the conductive plug is unevenly removed to define a second uppermost surface, at least a portion of which is disposed elevationally higher than a conductive line. In one aspect, conductive plug material can be removed by facet etching the conductive plug. In another aspect, conductive plug material is unevenly doped with dopant, and conductive plug material containing greater concentrations of dopant is etched at a greater rate than plug material containing lower concentrations of dopant.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with prior art methods.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown in Fig. 1.

Fig. 3 is an enlarged view of a portion of Fig. 2.

Fig. 4 is a view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 5 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 4.

Fig. 6 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 5.

Fig. 7 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 6.

Fig. 8 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 7.

Fig. 9 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 8.

Fig. 10 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 9.

Fig. 11 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown in Fig. 10.

Fig. 12 is a view of the Fig. 10 wafer fragment at a processing step in accordance with another embodiment of the invention.

Fig. 13 is a view of the Fig. 12 wafer fragment at a processing step subsequent to that shown in Fig. 12.

Fig. 14 is a view of either of the Figs. 11 or 13 wafer fragments, at a processing step subsequent to that shown in either of the respective figures.

Fig. 15 is a view of the Fig. 14 wafer fragment at a processing step subsequent to that shown in Fig. 14.

Fig. 16 is a view of the Fig. 14 wafer fragment at a processing step subsequent to that shown in Fig. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 4, a semiconductor wafer fragment in process in accordance with one embodiment of the invention is shown generally at 42 and comprises a semiconductive substrate 44. A pair of conductive lines 46 are formed over substrate 44 and comprise a polysilicon layer 48, a silicide layer 50 and an insulative cap 52. Sidewall spacers 54 are provided over conductive and non-conductive portions of lines 46. Lines 46 constitute a pair of spaced-apart, insulated conductive lines which define a node location 56 or surface area therebetween with which electrical communication is desired. In the illustrated and preferred embodiment, node location 56 comprises a diffusion region 57 to be connected with a bit line. Other node locations are defined by diffusion regions 57 laterally outward of node location 56, and comprise locations with which electrical communication with storage capacitors is desired, as will become apparent below. A first insulative layer 58 is formed over node location 56 and between the conductive lines. An exemplary material for layer 58 is BPSG.

Referring to Fig. 5, layer 58 is planarized as by chemical mechanical polishing to provide a generally planar upper surface 60. The planarization of layer 58 can be made to stop on or over the insulative caps of the conductive lines.

Referring to Fig. 6, a second layer of insulative material 62 is formed over node location 56 and has a generally planar upper surface 64.

Referring to Fig. 7, a patterned masking layer 66 is formed over substrate 44.

Referring to Fig. 8, openings 68 are formed through material of both first and second layers 58, 62 to proximate the node locations. Preferably, the openings are sufficient to expose the node locations over which each is formed.

Referring to Fig. 9, conductive material 70 is formed over the substrate, insulative material 62, and within openings 68. The openings are preferably filled with conductive material. An exemplary conductive material is polysilicon.

Referring to Fig. 10, conductive material 70 is planarized relative to insulative layer upper surface 64. Such isolates conductive material within openings 68 and provides planarized conductive projections 72 over the substrate. In the illustrated and preferred embodiment, conductive projections 72 constitute conductive plugs which are formed in connection with formation of DRAM circuitry. Individual conductive projections 72 include respective upper or uppermost surfaces 74 which

are joined with respective side surfaces 76. The side surfaces project away from the node location over which each is formed and terminate proximate the respective surface 74 with which it joins. Joinder between upper and side surfaces 74, 76 defines corner regions of the individual conductive projections. Intermediate and away from the corner regions of each projection is a central region 78.

Preferably and as shown, the individual conductive plugs project away from the respective node locations over which each is formed a distance which is further than a distance that one of the conductive lines projects away from the node location. Accordingly, each plug's uppermost surface is disposed elevationally over both conductive lines and is substantially coplanar with the generally planar portion of insulative material 62.

Referring to Fig. 11, corner regions of the conductive projections are beveled. In the illustrated example, the beveling of the corner regions comprises facet etching the conductive projection to provide the illustrated beveled construction. Such etching can take place in a cold wall processing chamber using an unheated chuck. Other conditions include a power setting of between 100 W to 600 W, a pressure setting of between 10 to 100 mTorr, and use of Argon ions preferably having incident angles of between 45° to 60°. The insulative material can be removed prior to the facet etching. Alternately, the insulative material can remain during the facet etching.

The facet etching of the conductive projection constitutes unevenly removing the conductive material sufficient to define a second uppermost surface 80, at least of portion of which is disposed elevationally higher than the conductive lines. In this example, more material is removed from the corner region than from the central region of each plug, and second uppermost surface 80 is generally non-planar.

Referring to Fig. 12, a second embodiment is shown, with the discussion proceeding with processing subsequent to the Fig. 10 wafer fragment. In this example, the conductive projections are unevenly doped proximate the upper and side surfaces. Such uneven doping can be accomplished using an angled ion implant at energies between about 20 keV to 1000 keV, and angles greater than 0° and less than about 60°. The angled ion implant subjects the corner regions to a greater degree of normal angle implanting such that greater implanting occurs relative to the corner regions as opposed to the upper surfaces. As a result, outermost side portions, e.g. the corner regions, of the conductive plug have greater concentrations of dopant than plug material therebetween proximate the central region. Insulative material 62 (Fig. 10) can be removed prior to doping the conductive plugs, or remain during the doping.

Referring to Fig. 13, the individual conductive plugs have been beveled. Such can be accomplished by etching material of the conductive plugs or projections containing greater concentrations of dopant at a greater rate than material of the conductive projections

containing lower concentrations of dopant. Insulative material 62 (Fig. 10) can be removed prior to the etching of the conductive plugs or remain during the etching. The beveling of the conductive plugs comprises unevenly removing material of the conductive plug to define a second uppermost surface 80a, at least a portion of which is disposed elevationally higher than the conductive lines. Exemplary etching can comprise dry or wet etching of the plug material. In the former, Cl_2 or HBr chemistries can be used to sufficiently activate etching of the corner regions. In the latter, wet etches with a sufficiently high pH can be used. Examples include TMAH or SCI (APM).

Referring to Fig. 14, a layer of material 82 is formed over the substrate, with BPSG being but one example.

Referring to Fig. 15, openings 84 are formed over the substrate and define a second alignment tolerance X_1 which is greater than the first alignment tolerance X (Fig. 3).

Referring to Fig. 16, conductive material 86 has been formed over, and is in electrical communication with the leftmost and rightmost conductive plugs and the respective diffusion regions over which the plugs are formed. Conductive material 86 constitutes respective storage node layers. Dielectric layers 88 are formed over the respective storage node layers 86, and a cell plate layer 90 is formed over the respective dielectric layers. Conductive material 94 is formed over, and is in electrical communication with the centermost conductive plug and the diffusion region over which it is formed. Conductive material 94

comprises a bit line. Here, the alignment tolerance between bit line contact material and adjacent storage capacitors is increased.

Advantages of the above-described methods and structures include that alignment tolerances can be increased with only a slight modification of the processing flow. Process viability can be improved for shifts which may occur in or during photo alignment. Additionally, the above methods allow scaling of contemporary technology to smaller generations of devices.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.